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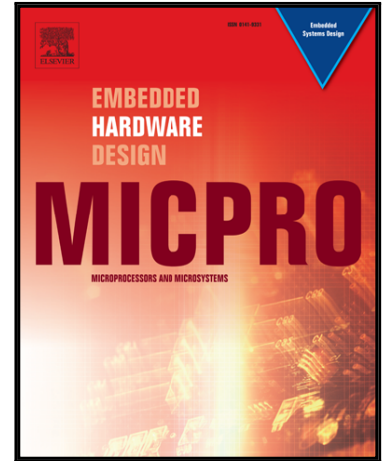
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## A Compact Digital Gamma-tone Filter Processor

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### Abstract

Area consumption is one of the most important design constraints in the development of compact digital systems. Several authors have proposed making compact Cochlear Implant processors using Gamma-tone filter banks. These model aspects of the cochlea spectral filtering. A good area-efficient design of the Gamma-tone Filter Bank could reduce the amount of circuitry allowing patients to wear these cochlear implants more easily. In consequence, many authors have reduced the area by using the minimum number of registers when implementing this type of filter. However, critical paths limit their performance. Here a compact Gamma-tone Filter processor, formulated using the impulse invariant transformation together with a normalization method, is presented. The normalization method in the model guarantees the same precision for any filter order. In addition, area resources are kept low due to the implementation of a single Second Order Section (SOS) IIR stage for processing several SOS IIR stages and several channels at different times. Results show that the combination of the properties of the model and the implementation techniques generate a processor with high processing speed, expending less resources than reported in the literature.

*Keywords:* Auditory models, Cochlear implant processor, Gamma-tone Filter

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## 1. Introduction

The development of digital artificial cochlear chips has attracted the interest of engineers for developing portable applications such as pitch detection, speech recognition and audio source localization on mobile devices, or for auditory prostheses [1]. These applications have used a model of the biological cochlea due to its capabilities for processing audio signals including natural sounds [2]. This cochlea functions as a transducer, converting the mechanical vibrations from the middle ear into electrical signals (auditory nerve spikes). These signals are sent to the human auditory system which responds to the information contained in the speech and audio signals.

Several studies show that the sound processing carried out by the cochlea, can be modeled using the over-complete Gamma-tone filter-bank, due to its resemblance to the human auditory system [2],[3]. In addition, recently proposed mathematical models, reported in the literature, show that Gamma-tone filter banks designed using the impulse invariant transformation allow digital implementation of the analogue cochlea while employing reasonable computation with negligible distortion [4]. The hardware implementation of the cochlea, whether analogue or digital, is called an *artificial cochlea* chip or *silicon cochlea*, [5]. Because an efficient Cochlea chip is very important in several fields, the development of efficient cochlea chips has been an active research field. One of the first analogue silicon cochleae was developed by Lyon and Mead [4], using analogue VLSI  $3\ \mu\text{m}$  technology. It is reported that this cochlea chip, implemented using a cascade of 480 bi-quad filter sections, provides similar behavior than the human cochlea. A silicon cochlea which provides a good approximation of the human cochlea was proposed by Mandal et.al. [6]. One of the most recent approaches was focused on building a bio-realistic analog CMOS Cochlea with high tunability and ultra-steep roll-off. The Chip response has high fidelity with respect to physiological experiments on mammalian cochlea and is  $0.9\ \text{mm}^2$  in area and consumes  $59.5 \sim 90.0\ \mu\text{W}$  [7].

Analogue implementations of artificial Cochlea chips, such as the above, are

potentially efficient in terms of processing speed and area when compared with the digital implementations. However, the analogue approach is susceptible to other factors, such as temperature, transistor mismatch and power supply noise [7]. To solve these problems several digital implementations of cochlear chips  
35 have been proposed aiming for efficient sound processors with minimal area. One of the critical factors to be considered in the development of artificial cochlea chips is the precision of the variables of the system. This factor has been taken into account in the system proposed by Van Immersel and Peters [8], which supports the emulation of the biquadratic filters with arbitrary precision and  
40 uses a scaling of the fixed-point precision as a method to avoid overflow. In [9], a cochlea chip is designed to work in real-time data maximizing the use of Hardware resources.

This paper proposes a digital cochlear processor based on a digital Gamma-tone filter bank to improve the area compared to existing digital designs. Our  
45 strategy maximizes the utilization of a single SOS stage to implement any SOS stages and several channels employing a time multiplexing technique. Indeed, the use of the impulse invariant transformation and the application of the normalization method to the filter coefficients allow creating an efficient filter bank processor in terms of processing speed and area resources, respectively.

50 Evaluation results are provided to show the desirable properties of the proposed system. The rest of the paper is organized as follows. Section 2 presents the gamma-tone filter bank model. Section 3 presents the overview of the Gamma-tone Filter Processor. Evaluation results are provided in Section 4. Section 5 shows the improvement achieved by our proposal when compared  
55 with the current approaches. Finally Section 6 provides the conclusion of this work.

## 2. Review of the Gamma-tone Filter Bank

Gamma-tone filters are defined in the continuous time domain, and can be mathematically modeled, in the discrete time domain, using different tech-

60 niques of digital signal processing such as the impulse invariant transformation, the Z-matched transform and the bilinear transform. To select an appropriate transformation, in addition to the computational complexity, the introduced distortion must be considered. To this end, several works [8], [10],[11] show that the model employing the impulse invariant transformation provides the best  
65 performance because it has a low computational cost and lower distortion when compared with the Z-matched and bilinear transformations. Thus according to the previous published works [8] [11] the impulse response of a Gamma-tone filter of order  $\alpha$ , is given by the product of a gamma function multiplied by a cosine function, as follows:

$$\psi_{f_c}^\alpha(t) = \frac{1}{(\alpha-1)!} t^{\alpha-1} e^{-2\pi b_m t} \cos(2\pi f_c t) u(t) \quad (1)$$

70 where  $\alpha$  is the filter order,  $b_m$  is the  $m$ 'th filter bandwidth in Hz and  $f_{cm}$ , is the resonance frequency. Next using the Euler representation of cosine function in eq. 1 and taking the Laplace transform of the resulting equation, after some manipulations it follows that the transfer function of the  $m$ 'th gamma-tone and pass filter  $H_m(s)$  can be represented in terms a cascade of  $\alpha$  second order band  
75 pass filters as follows [8], [10],[11]:

$$H_m(s) = \left( \frac{K(s + 4\pi b_m)}{(s + 2\pi b_m - j2\pi f_{cm})(s + 2\pi b_m + j2\pi f_{cm})} \right)^\alpha \quad (2)$$

Because the proposed system will be implemented in the discrete time domain, eq. 2 must be transformed to the z-domain. To this end, the impulse invariant transform is used because it provides a discrete time version of eq. 2 with less frequency distortion as compared with the bilinear and Z-matched  
80 transforms. Thus, applying the impulse invariant transform to eq. 2, it follows that

$$H_m(z) = \left( \frac{2 - 2B_m z^{-1}}{1 - 2B_m z^{-1} + C_m z^{-2}} \right)^\alpha, \quad (3)$$

where

$$B = e^{-2\pi b_m T} \cos(2\pi f_{cm} T) \quad (4)$$

$$C_m = e^{-4\pi b_m T} \quad (5)$$

As shown in eq. 3 the Gamma-tone filter transfer function, can be obtained as a cascade of  $\alpha$  filters of second order with complex conjugated poles. Thus it is important to normalize the gain of each stage because it allows us to factorize the transfer function of the gamma-tone filter in  $\alpha$  identical SOS stages. This avoids the recalculation the filter coefficients when the value of  $\alpha$  is changed. To this end, because each stage represents a second order band pass filter transfer functions, consider the frequency response of a second stage evaluated in  $2\pi f_{cm}$ , which is given by

$$H_m(f_{cm}) = H_m(z)|_{Z=e^{j2\pi f_{cm}}} = \frac{2 - 2B_m z^{-1}}{1 - 2B_m z^{-1} + C_m z^{-2}} \Big|_{Z=e^{j2\pi f_{cm}}} \quad (6)$$

where  $f_{cm}$  is the resonance frequency. Thus from eq. 6 it follows that

$$H_m(f_{cm}) = \frac{2 - 2B_m e^{-j2\pi f_{cm}}}{1 - 2B_m e^{-j2\pi f_{cm}} + C_m e^{-j4\pi f_{cm}}}, \quad (7)$$

whose magnitude is given by

$$|H_m(f_{cm})| = \sqrt{\frac{(2 - 2B_m \cos(2\pi f_{cm}))^2 + 4B_m^2 \sin^2(2\pi f_{cm})}{(1 - (2B_m + C_m) \cos(2\pi f_{cm}))^2 + (2B_m + C_m)^2 \sin^2(2\pi f_{cm})}}. \quad (8)$$

Thus normalizing the magnitude of  $H_m(f_{cm})$ , from eqs. 3 - 5 and 8 it follows that

$$H_m^N(z) = \left( \frac{A_m^N - B_m^N z^{-1}}{1 - 2B_m z^{-1} + C_m z^{-1}} \right)^\alpha, \quad (9)$$

where

$$A_m^N = \frac{2}{|H_m^N(f_{cm})|} \quad (10)$$

and

$$B_m^N = \frac{2e^{-2\pi b_m T} \cos(2\pi f_{cm} T)}{|H_m^N(f_{cm})|} \quad (11)$$

Next the normalized filter coefficients,  $A_N$  and  $B_N$ , provide the SOS stages with gain equal to one. Finally taking the inverse  $Z$ -transform of eq. 9 we obtain the output of the gamma-tone filter which is given by

$$y_i(n) = A_i^N y_{i-1}(n) - B_i^N y_{i-1}(n-1) + 2B_i y_i(n-1) - C_i y(n-2) \quad (12)$$

100 The above synthesis method provides a systematic procedure that allows the implementation of the Gamma-tone filter by cascading identical second order stage independently on the value of  $\alpha$ . It is important because it is known that the order of Gamma-tone filter can vary depending on the application and the type of signals to be processed.

105 Thus, because the filter can be implemented or represented by a cascade of SOS IIR band pass filters, if a given application requires the implementation of a Gamma-tone filter with  $\alpha = 4$  it is necessary to use four SOS IIR band pass filters connected in cascade as shown in 1, where each block represents an second order IIR filter. Consequently the value of  $\alpha$  is equal to the number of SOS stages  
110 required for implementing the Gamma-tone filter. Therefore to implement the Gamma-tone filter it would be necessary to calculate the coefficients for each stage depending on the value of  $\alpha$ . However using the mathematical model described above together with the normalization procedure, the calculations can be reduced because in this situation it is only necessary to calculate the  
115 coefficients of the first stage, because the same coefficients can be used in the synthesis of later stages, reducing the computational cost and storage.

### 2.1. Design Parameters for the Gamma-tone Filter Bank

According to eq. 2 when the ear is stimulated with a given sound, different regions of the basilar membrane respond according to the frequency of the  
120 sound. These regions can be considered as a bank of cochlear filters along the



basilar membrane. Because the Gamma-tone filter accurately models the basilar membrane, several studies have been carried out to determine its optimum parameters in terms of the Bark frequency scale. Thus depending on the sampling frequency, the maximum number of second order band pass filters is given  
 125 by

$$N_{max} = \left\lceil 7Ln \left( \frac{f_s}{1300} + \sqrt{\frac{f_s}{1300}} \right)^2 + 1 \right\rceil \quad (13)$$

where  $[x]$  denotes the integer part of  $x$ , the resonance frequency is given by

$$f_{cm} = 325 * \frac{e^{2m/7}}{e^{2m/7}} \quad (14)$$

$$b_m = 25.1693 \left( 4.37 \frac{f_{cm}}{1000} + 1 \right) \quad (15)$$

is the bandwidth of the  $m$ 'th band pass filter used in (11) to estimate  $B_m^N$ . Thus, taking into account that the human voice roughly has a range of frequencies from 100 Hz to 4000 Hz, designing a Gamma-tone filter bank with different  
 130 values of  $\alpha$  and 16 channels that emulates the cochlear human ear filter bank gives the resonance frequencies shown in the Table 1. It is worth noting that our approach potentially allows selecting frequencies to detect the onset of the sound [12], employing the same mechanisms described above.

### 3. Overview of the Gamma-tone Filter Processor

135 The cochlea processor consists of a single SOS IIR stage, an array of internal Block RAMs and Control Unit, as shown in Fig. 3. A single SOS IIR stage is used as a part of the proposed processor to compute any filter order per channel and several channels employing the same precision in the whole system. Two design criteria have helped to build the compact processor with a single  
 140 SOS IIR stage. The first is related to the technique of time multiplexing (well known as a virtualization concept) to process different virtualized SOS stages and virtualized channels at different instances of time using a single physical SOS

during the sample time  $T_s$ . The second is focused on the utilization of Block RAMs. Our proposal maximizes the use of Block RAM, which is contained  
 145 in the FPGA, to achieve the minimum consumption of Registers and LUTs. Modern FPGAs feature a large number of low-area BRAMs, which can store up to 36 Kbits each. In our approach, these BRAMs store the values of the internal variables ( $w_0$  and  $w_1$ ) of each SOS and the coefficients ( $A_N$ ,  $B_N$ ,  $B$  and  $C$ ) for each channel. The number of BRAMs to store the internal variables ( $w_0$  and  $w_1$ )  
 150 of the virtualized IIR stages is a function of the number of channels and the size of each BRAM is determined by the number of virtual SOS stages. Finally, the Control Unit is responsible for synchronizing the reading and writing operations of the BRAMs enabling the internal variables ( $w_0$  and  $w_1$ ) and coefficients ( $A_N$ ,  $B_N$ ,  $B$  and  $C$ ) of their corresponding virtualized SOS IIR stage to be processed  
 155 by the physical SOS IIR stage.

The SOS IIR stage is composed of four  $16 \times 16$  bit multipliers, two adders and two Flip-Flops, as shown in Figure 4. The coefficients ( $A_N$ ,  $B_N$ ,  $B$  and  $C$ ) are loaded from the BRAM coefficients into registers ( $A_N$ ,  $B_N$ ,  $B$  and  $C$ ) in order to be updated when a particular channel is processed. Likewise, the  
 160 flip-flops store the internal variables ( $w_0$  and  $w_1$ ) when the *load\_ff* signal is set high (see Fig. 5). In this case, internal variables ( $w_0$  and  $w_1$ ) must be stored back after they are updated when a specific virtualized SOS stage is calculated.

As can be observed from Fig. 3, the Control Unit has an interface with the external CPU in order to load the coefficients to the BRAM. This data interface  
 165 uses Gigabit-Ethernet. The user sends the coefficients, which are previously calculated, through an MSDOS command script. Once the coefficients are loaded in the BRAM coefficients, the Control Unit distributes serially the value of the variables ( $w_0$  and  $w_1$ ) to each virtualized IIR stage reading its corresponding block of BRAM memory. The waveform diagram, which is obtained with the  
 170 ModelSim<sup>®</sup> software, shows the signals to control the BRAMs and the internal registers of the SOS IIR stage. As can be observed from Fig. 5, the time multiplexing technique can be applied because the sample duration is longer than the system clock time, allowing the calculation of every channel by its respective

SOS IIR stages. Every SOS IIR stage is processed by the physical SOS IIR stage  
 175 serially as shown in Fig. 5. For example, the right side of the waveform diagram  
 of Fig. 5 shows the signal *Address\_a*. This signal represents the address of the  
 BRAM internal variables ( $w_0$  and  $w_1$ ) for each SOS of the first Channel (see  
 Fig. 3). Once these SOS stages are processed the next internal variables ( $w_0$   
 and  $w_1$ ) of the SOS stages, which correspond to channel 2, are loaded by setting  
 180 the signal *load\_ff* high, and the *address\_coe* is set to 1 to load the coefficients  
 ( $A_N$ ,  $B_N$ ,  $B$  and  $C$ ) into internal registers of the SOS IIR stage, as shown in  
 Fig. 3.

An important factor to be defined is related to the maximum number of  
 times or maximum number of virtualizations during a single Sampling Clock  
 185 Cycle. The maximum number of virtual IIR stages can be found from equation  
 16:

$$T_s > (N_p * N_{SOS} * N_C) * T_{clk} \quad (16)$$

where  $T_s$  is the sampling time,  $N_p$  are the number of clock cycles to process a  
 single virtualized SOS IIR stage,  $N_{SOS}$  is the number of virtual SOS mudules,  
 $N_c$  is the number of channels, and  $T_{clk}$  is the time of the clock system.

#### 190 4. Simulation and Implementation and Results

To verify the proposed method some filter banks were designed. The fil-  
 ters obtained were simulated in MatLab<sup>®</sup> to verify their response using 64 bit  
 floating point precision and then implemented on a Field Programmable Gate  
 Array (FPGA) employing 16 bit fixed point. The next sub-sections compare  
 195 the response of the filter bank using these two representation methods..

##### 4.1. MatLab simulation results

The filter bank was implemented as a cascade of SOS IIR filters. The center  
 frequencies of the 16 channels Gamma-tone filter are shown in Table 1.

Figure 6 shows the frequency response of a SOS Gamma-tone filter obtained  
 200 in Matlab, where the filter coefficients were designed using 64-bit floating point  
 numbers and the sampling frequency was 16 KHz.

In order to do a simpler implementation on the FPGA the filter coefficients  
 were converted to 16-bit integers, and the frequency response of this filter bank  
 is shown in the Figure 7. The results show that the integer representation does  
 205 not change the response. To verify this a cascade of SOS was added to increase  
 the order of the filters.

Figure 7 shows the frequency responses of Gamma-tone filters with order  
 16 and 24 (equivalent to 8 SOS and 12 SOS), respectively. From the results it  
 can be seen that increasing the filter order improves the selectivity, so that the  
 210 stopband approaches its ideal characteristics.

The simulation results demonstrate that the filters with higher orders im-  
 prove the stopband attenuation. Further, the integer representation of the coef-  
 ficients does not change the response of the channels, and the center frequencies  
 and bandwidth are not altered.

#### 215 4.2. Implementation on a Kintex7 FPGA

The Filter Bank processor prototype was implemented on the *KC705* board  
 kit which includes a *Xilinx Kintex7* FPGA. The Gamma-tone filter banks de-  
 signed with 16-bit integer coefficients were implemented on the FPGA, and the  
 frequency responses of the filters implemented were obtained with an *HP4395A*  
 220 network analyzer. The fixed-point operators (multiplier and adder) were carried  
 out by means of LUTs in order to increase the processing speed. Figure 8 shows  
 an arbitrary example that represents the response of the fourth channel centered  
 at  $209.13\text{Hz}$  for filters with order  $\alpha = 4, 16$  and  $24$ . As can be seen from this ex-  
 ample, the higher order filters clearly provide much higher selectivity. Similarly,  
 225 the selectivity response for other channels improves as the value of  $\alpha$  increases.  
 For a better visualization of the frequency responses of all the channels, the  
 results obtained from the network analyzer were plotted in Matlab, the results  
 are shown in the Figure 9.

The results show that a simple implementation of Gamma-tone filter bank  
 230 processor with higher order can be made. The only step required is to add  
 cascade sections of the same coefficients, namely, increase the number of vir-  
 tualized IIR stages. The frequency centers are not altered and the selectivity  
 is improved,. The bands corresponding to the  $F_c = 100Hz$  and  $127 : 88Hz$  ex-  
 235 hibit a small gain that is less than  $3dB$  for the 16'th-order filter and  $AdB$  for  
 the 24'th-order filter, which is not significant. The center frequencies of the other  
 channels are around  $-1dB$ , which could be due to the connections between the  
 board and the network analyzer.

In addition to the implementation of the 16-bit fixed-point implementation,  
 the proposed Gamma-tone filter bank processor was designed with 16-bit float-  
 240 ing point and implemented on a Kintex-7 board in order to compare them.  
 Clearly, the area required for implementing 16-bit floating point operators us-  
 ing LUTs and registers is greater than that for the 16-fixed-point operators (see  
 Table 6). Figure 10 shows the frequency response of an arbitrary channel that  
 is centered at  $209.13Hz$  for filters with order  $\alpha = 4$ . As can be observed from  
 245 Fig. 10, the frequency responses are quite similar using both techniques (16-bit  
 fixed-point and 16-bit floating-point). It is worth noting that the frequency  
 responses of the remaining channels were not dissimilar.

## 5. Related Work

Our proposal was tested with a single SOS stage processing twelve virtual-  
 250 ized SOS IIR stages per channel and sixteen channels on the *Kintex-7* board  
 prototype. Theoretically, the processor is capable of computing twelve-SOS IIR  
 stages per Channel and one hundred and fifty channels. These figures were  
 calculated by replacing the above parameters in the equation 16, as shown in  
 Table 2.

255 As can be observed from Table 2, the current implementation and the the-  
 oretical values met the condition. This illustrates the tradeoff of the proposed  
 system between the number of SOS IIR stages and number of channels to be

calculated by the processor during a sample clock cycle.

Table 3 shows a comparison between the conventional and our proposal in terms of the number of functional units and the number of registers. As can be observed from Table 3, the implementation of the SOS IIR stage further requires four registers while keeping the same number of functional units.

Table 4 compares the units required to implement the conventional SOS stages and the proposed system to process twelve-SOS IIR stages per channel and sixteen channels. The use of this technique allows improving the area consumption by a factor of 192, 192 and 64 for adders, multipliers and number of registers, respectively.

Several works attempt to emulate the artificial cochlea chip while consuming a minimum of hardware. In this section, we present a comparative analysis between our proposal and other approaches in terms of area consumption (LUTs and registers). The results of the obtained analysis are shown in Table 5.

The condition, which is given by equation 16, could be met for the case of requiring the implementation of 88 SOS stages per channel and seventeen channels, as shown in Table 8, expending  $47.8\mu s$  taking into account the following parameters:  $T_s = 62.5\mu s$ ,  $N_P = 4$  clock cycles,  $N_{sos} = 88$  SOS IIR stages,  $N_c = 17$ , and  $T_{clk} = 8\mu s$ . Under this condition, the designed Gamma-tone filter processor could achieve a 94% and 99% reduction in consumption of LUTs and registers, respectively, when compared to [11]. In conclusion the Gamma-tone processor expends the same number of LUTs and registers to implement a range of channels from 16 to 150 and twelve-SOS IIR stage per channel meeting the condition given by equation 16. Table 8 shows the calculated processing time for implementing all the mentioned approaches [13], [9], [11], [10] using our strategy. As can be observed from Table 8, all the required processing time are under  $T_s = 62.5\mu s$  making feasible the application of our strategy under the design parameters of mentioned approaches.

All the discussed implementations use fixed-point operators to emulate the Gamma-tone filter banks. Where 16-bit floating-point operators, which are built into LUTs and registers, are used, the area consumption is increased as shown

in Table 6. This table shows the area consumption required to implement a  
 290 single adder and a single multiplier under two formulaic representations (16-bit  
 fixed-point and 16-bit floating point). Table 6 shows clearly that the required  
 number of LUTs to implement the 16-bit floating-point multiplier and 16-bit  
 floating-point adder is increased by a factor of 10 and 5 when compared with  
 their counterparts, respectively. In addition, the floating-point operators require  
 295 registers which are not needed for the fixed-point operators.

The number of LUTs and registers required to implement 16-bit floating-  
 point twelve-SOS IIR stage per channel and sixteen channels with the conven-  
 tional method is shown in Table 7. For this example, the required LUTs and  
 registers are 733,824 and 1,136,952, respectively. These values have been calcu-  
 300 lated using the data of Table 4 and 6, which exceed the available resources on  
 the current FPGA (203,800 LUTs and 407,600 registers). Therefore, this makes  
 their implementation on the Kintex-7 XG7K355T board infeasible.

## 6. Conclusions and Future work

A virtualizable Gamma-tone filter bank processor, which can be used for  
 305 emulating human auditory models using the minimum constrains, has been de-  
 veloped. This electronic artificial cochlear chip demonstrates the efficient use of  
 the available embedded resources in the FPGA with the help of the normaliza-  
 tion method applied to the mathematical model to create compact systems. An  
 important factor, which was taken into account to create this processor, is the  
 310 precision of the variables of the system. The results show better performance  
 regarding the selectivity of the filter bank when increasing the filter order using  
 16 bits. The proposed normalization of the Gamma-tone filter and the imple-  
 mentation strategy guarantee the minimum area consumption. Additionally,  
 the power consumption of the proposed Gamma-tone filter processor was esti-  
 315 mated using the VIVADO tool v2014.1. The obtained power consumption is  
 around 5 mW to 250 mW depending on the number of BRAMs per channel.  
 Part of our future work is the fabrication of a full custom implementation, which

potentially allows further reduction of the power consumption of our processor.

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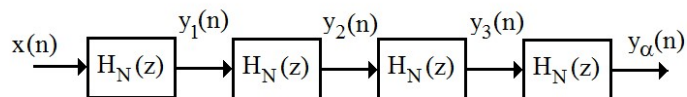


Figure 1: Block diagram of the Gamma-tone structure implemented as a cascade of SOS IIR identical stages.

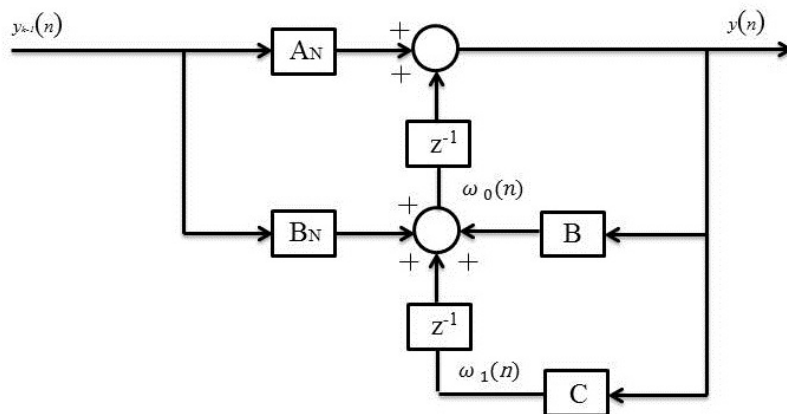


Figure 2: Block diagram of the SOS IIR stage of the Gamma-tone filter.

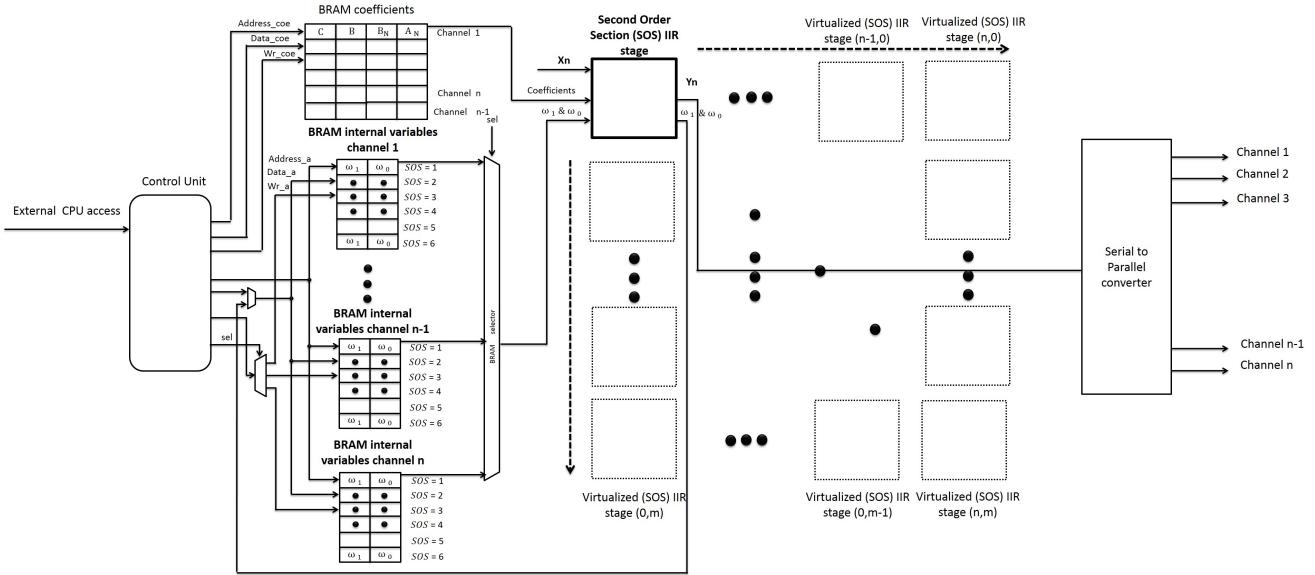


Figure 3: Scheme of the proposed IIR biquadratic filter of order  $n$  with  $m$  channels .

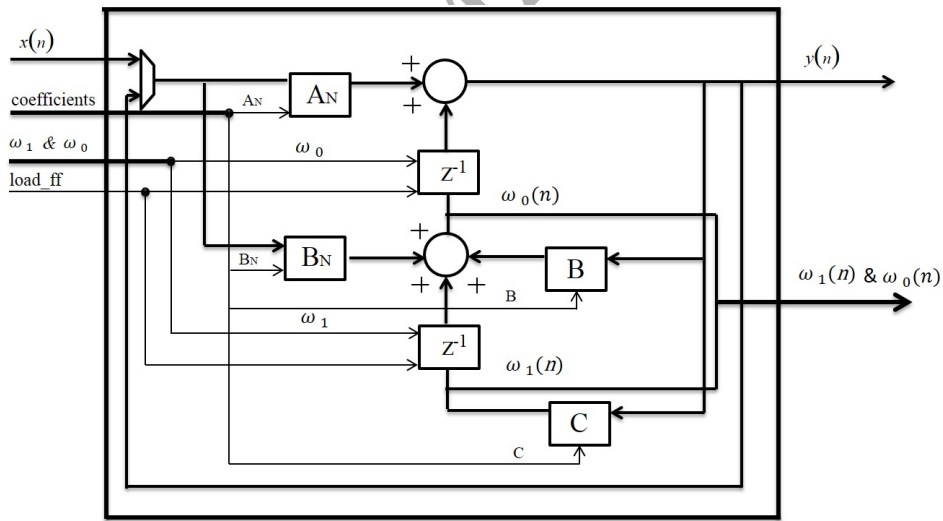


Figure 4: Scheme of the structure of the SOS stage.

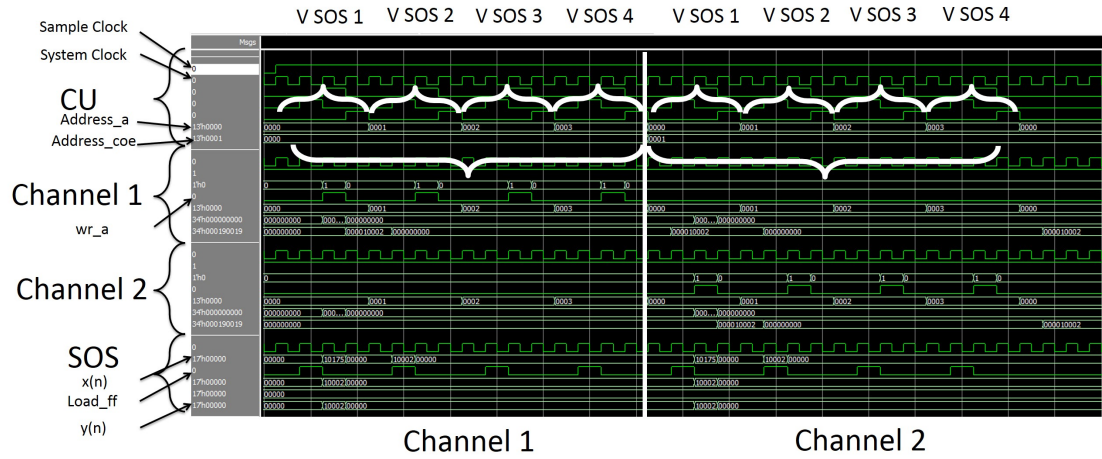


Figure 5: Scheme showing the structure of the SOS stage.

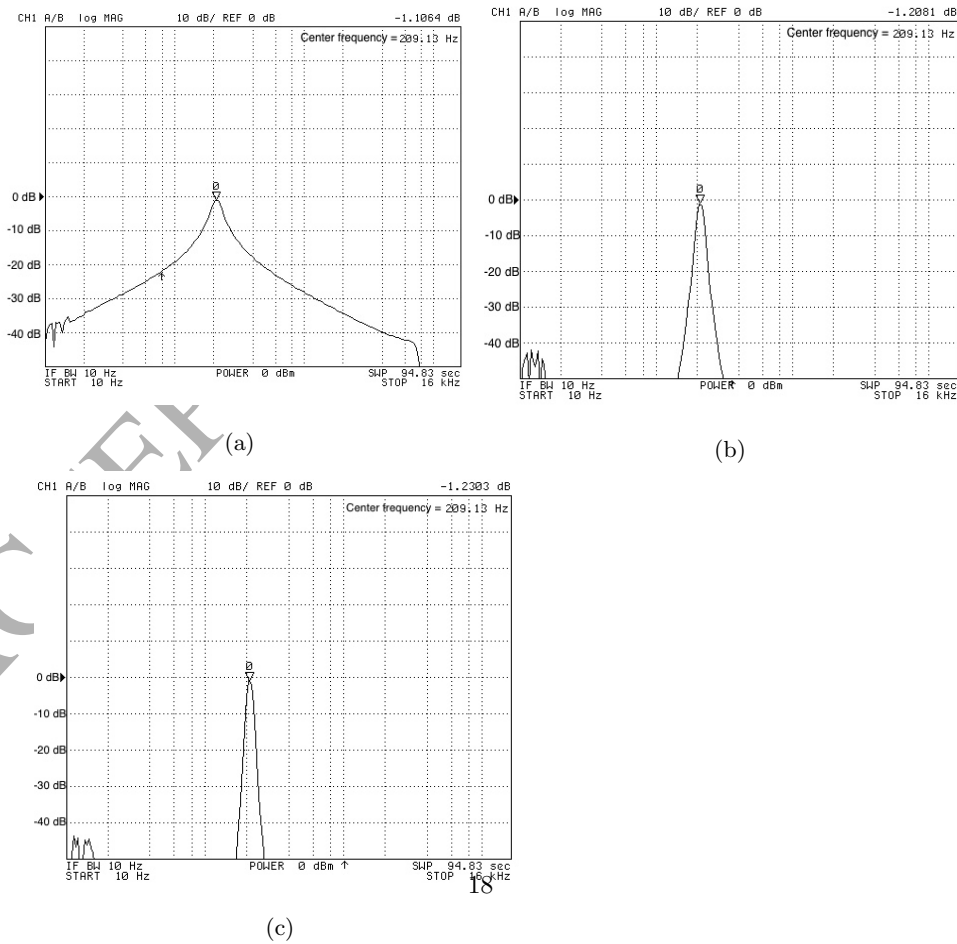


Figure 8: Frequency responses of the fourth channel obtained with a network analyzer, a Second-order filters, b 16'th-order filters, c 24'th-order.

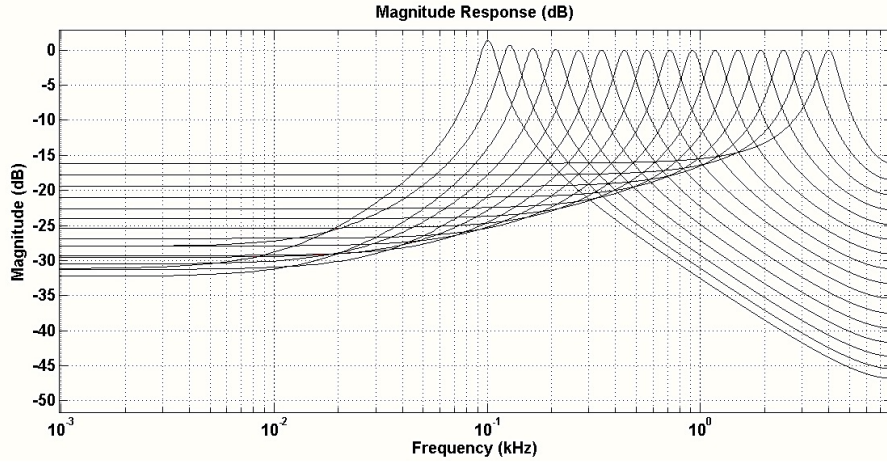
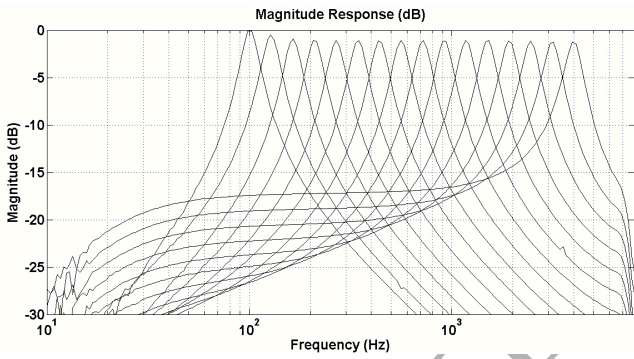
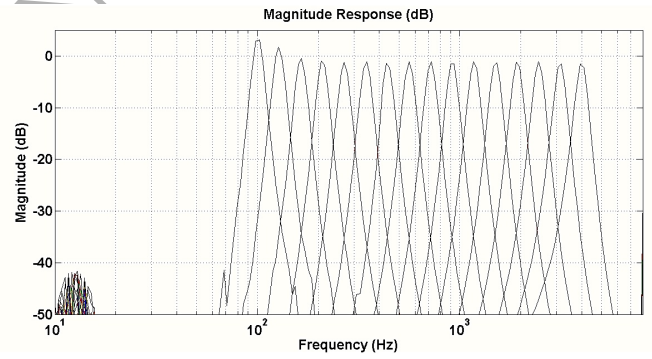


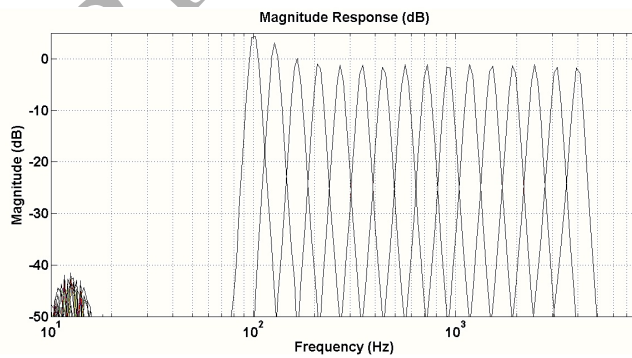
Figure 6: Frequency response of the Gamma-tone filter using 64-bit floating point numbers



(a)



(b)



(c)

Figure 9: Frequency responses of 16 bands of the Gamma-tone filter bank processor implemented on a Kintex-7 board, a Second-order filters, b 16'th-order filters, c 24'th-order.

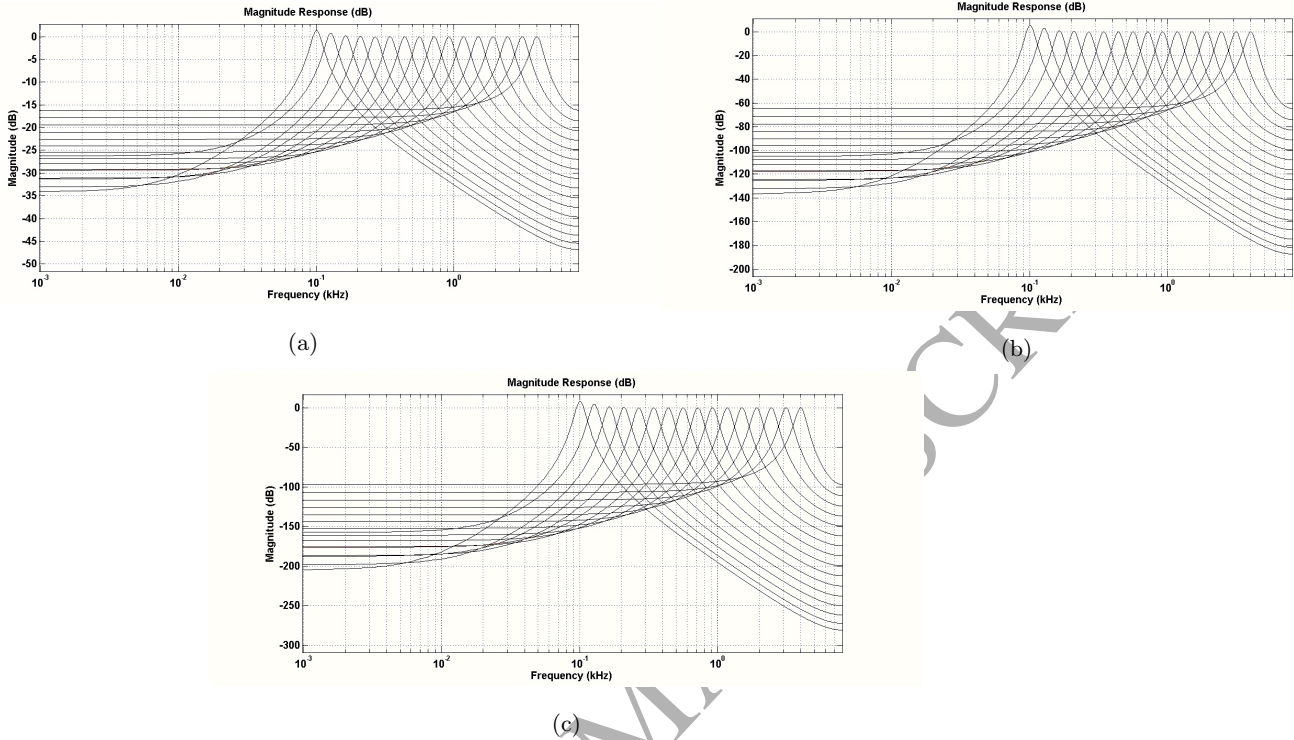


Figure 7: Frequency responses of 16 channel Gamma-tone filters, a Second-order filters, b 16<sup>th</sup>-order filters, c 24<sup>th</sup>-order.

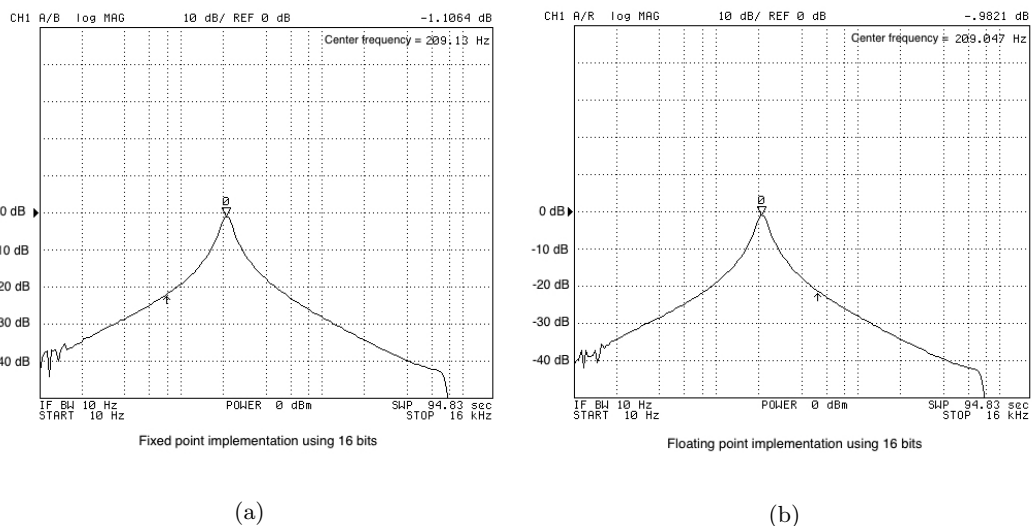


Figure 10: Frequency responses of the fourth channel obtained with a network analyzer, a Second-order filters implemented with 16-bit fixed-point operators, b Second-order filters implemented with 16-bit floating-point operators.

Channels	1	2	3	4	5	6	7	8
$F_c(Hz)$	100	127.88	163.53	209.13	267.43	342	437.34	559.28
Channels	9	10	11	12	13	14	15	16
$F_c(Hz)$	715.21	914.61	1169.61	1495.70	1912.70	2445.97	3147.92	4000

Table 1: Center frequency of 16 channel Gamma-tone filter

<p>The current version  <math>(T_s = 62.5\mu s, N_P = 4clockcycles</math>  <math>N_{SOS} = 12</math> SOS IIR stages,  <math>N_c = 16</math> and <math>T_{clk} = 8ns)</math></p>	$62.5\mu s > 6.14\mu s$
<p>Theoretical Values  <math>(T_s = 62.5\mu s, N_P = 4clockcycles</math>  <math>N_{SOS} = 12</math> SOS IIR stages,  <math>N_c = 150</math> and <math>T_{clk} = 8ns)</math></p>	$62.5\mu s > 57.6\mu s$

Table 2: Calculation of the performance of the current implementation and the theoretical figures

Approach	Number of functional Units		Number of Registers
	Adders	Multipliers	
Conventional	2	4	2
This Work	2	4	6

Table 3: Comparison between conventional and the proposed SOS IIR stage.

Approach	Number of functional Units		Number of Registers
	Adders	Multipliers	
Conventional	384	768	384
This Work	2	4	6

Table 4: Comparison between conventional and the proposed SOS IIR stage implementing twelve-SOS IIR stages per channel and sixteen channels.

Approach	Number of Channels	Word Length (bits)	Number of SOS IIR stages	Order ( $\alpha$ )	Number of LUTs	Number of Registers
This work	16-150	16	12	24	646	85
Mishra [13]	12	8, 21	5	10	751	445
Brucke [9]	30	16, 18, 20, 22, 24, 26, 28, 30	2	4	2800	5600
Leong [11]	17	10, 12, 16, 24, 32	88	176	10771	21542
Dundur [10]	16	8, 12, 14, 16	1-4	2-8	20699	823

Table 5: Comparison between the presented work and other approaches

Operator	Resources (16-bit floating-point operators)		Resources (16-bit fixed-point operators)	
	LUTs	Registers	LUTs	Registers
Adder	379	602	67	0
Multiplier	766	1,238	73	0

Table 6: Comparison between 16-bit fixed-point operators and 16-bit floating-point operators in terms of area consumption.

Approach	Resources	
	LUTs	Registers
Conventional (16-bit floating-point)	733,824	1,136,952
This Work (16-bit fixed-point)	426	0

Table 7: Comparison between conventional method (using 16-bit floating-point operators) and the proposed method (using 16-bit fixed-point operators) implementing twelve-SOS IIR stages per channel and sixteen channels in both cases.



Number of Channels	Number of SOS IIR stages	Processing time ( $\mu s$ )
12	5	1.92
30	2	1.92
17	88	47.88
16	1-4	0.5, 1, 1.5, 2

Table 8: Processing time for implementing a variety of channels and SOS stages using the proposed strategy



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